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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,073	01/14/2004	Chih-Chieh Yeh	87092291.242025	4123

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BAKER & MCKENZIE
PATENT DEPARTMENT
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EXAMINER	
NGUYEN, TAN	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,073	YEH ET AL.	
	Examiner	Art Unit	
	Tan T. Nguyen	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8/11/04; 10/5/04;
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The Information Disclosure Statements submitted by Applicants on January 14, 2004, October 1 and 5, 2004 have been received and fully considered.

2. The drawings are objected to because in Figure 4C, "V_{b1}-V_{b4}" should be changed to --V_{d1}-V_{d4}--. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

Applicants failed to provide adequate written description of how the electrons migrate toward and retained in the trapping layer when a positive voltage is applied to

the base and a negative voltage is applied to the gate. The electrons move from negative voltage to positive voltage.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato et al. (U.S. Patent No. 5,576,995) in view of Wang et al. (U.S. Patent No. 6,331,953).

Sato et al. disclosed in Figure 1 a memory cell of a flash memory includes a P-well [8], a floating gate [2], a control gate [6], a drain and source [7] (column 7, line 65 to column 8, line 10). Sato et al. disclosed a third method in that the writing is operated by release of electron from the floating gate with FN (Fowler-Norheim) current cause by applying 0V to the P-substrate, making source open, applying a high negative voltage (-12V) to the control gate and a relative high positive voltage (+5V) to the drain. Regarding claims 13-14, since a high negative voltage applied to the control gate and a positive voltage applied to either the drain or source, it inherently causes the electrons migrate from the floating gate to the drain or the source, or would cause the electric holes migrate to the floating gate. Regarding claim 1, Sato et al. also disclosed by the third method, the erasing operated by injection of electrons with FN current into the floating gate from a channel in the substrate which is induced by applying 0v to the

substrate and the source, making the drain open, and applying a high positive voltage (+18v) to the control gate (column 2, line 54 to column 3, line 5).

Sato et al. did not discuss the step of evaluating a read current after the erase or program operation, and repeating the step of applying a voltage bias between the base and the gate (verifying operation).

Regarding claim 1, Wang et al. disclosed in Figure 6 a second erase technique in which after the cell is erased, the cell is read to determined if the cell has been erased. If it has not, the cycle is repeated until the cell is erased (Column 12, line 59 to column 13, line 1). Furthermore, although Sato et al did not discuss a negative voltage is applied to the base, it is known in the art that negative voltage has been applied to the substrate in erase operation.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the erasing method disclosed by Sato et al. by providing the verify operation of Wang et al., and instead of applying 0V to the substrate, it would have been obvious to apply a negative voltage to the substrate in the erase operation.

The rationale is as follows: A person of ordinary skill in the art would have been motivated to use the verify operation of Wang et al. to check whether the memory has been erased completely, and by applying negative voltage to the substrate, it would reduce the high positive voltage applied to the control and still effectively inject electrons to the floating gate in the erase operation.

Regarding claims 4-11, Wang et al. disclosed different erase techniques in which either the drain voltage remains constant and the gate voltage is ramped (Figure 7), or

the gate voltage remains constant while the drain voltage is ramped (Figure 9) during the erase verify operation.

Regarding claim 12, Sato et al. disclosed in TABLE 3 (column 2), a read operation in which a positive voltage (+5v) is applied to the control gate, a second positive voltage (+2v) is applied to the drain, and the source is grounded.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the erase operation of Sato et al. by varying the voltages applying to the gate, the drain of the cell as Wang et al. disclosed. It also would be obvious to replace the voltage applied to the drain with negative voltage applied to the substrate in the erase operation as known in the art (U.S. Pat. No. 6,344,995, Abstract).

The rationale is as follows: A person of ordinary skill in the art would have been motivated to vary the voltages applying to the control gate and the substrate of the selected cell by ramping the voltages to optimize the erase operation.

6. Claims 13-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato et al. in view of Wang et al. and Yiu et al. (U.S. Patent No. 5,526,307).

See descriptions of Sato et al. and Wang et al. in paragraph 5, supra. Sato et al. and Wang et al. did not disclose the step of setting the memory cell to an initial state of a first gate threshold voltage.

Yiu et al. disclosed in Figure. 4A a flow chart of a program operation in which to begin the program operation, a sector into which data is to be program is erase (block 600), then the program potential are applied to the segment being programmed (block

605), and after the program operation, a verify operation is executed (block 606) (column 11, lines 41-59).

Regarding claim 13, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the program operation disclosed by Sato et al. by providing the operation of erasing at the beginning and the verify operation after the program operation.

The rationale is as follows: A person of ordinary skill in the art would have been motivated to erase the memory cells before the program operation to make the memory cells have uniform data state, and to use the verify operation to make sure the memory cells have been programmed completely.

Regarding claim 14, Sato et al. disclosed in the program operation, a negative voltage (-12v) is applied to the control gate, and a positive voltage (+5v) is applied to the drain (column 2, lines 62-67).

Regarding claims 15-22, Wang et al. disclosed different erase techniques in which either the drain voltage remains constant and the gate voltage is ramped (Figure 7), or the gate voltage remains constant while the drain voltage is ramped (Figure 9) during the erase verify operation. How the erase voltages in erase operation are ramped in Wang et al. would be used to ramp the voltages applied to the control gate and the drain (source) as well.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the erase operation of Sato et al. by varying the voltages applying to the control gate, the drain (source) of the cell as Wang et al. disclosed.

The rationale is as follows: A person of ordinary skill in the art would have been motivated to vary the voltages applying to the control gate and the drain (source) of the selected cell by ramping the voltages to optimize the program operation.

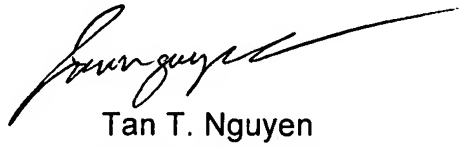
7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Caravella et al. and Lee are cite show memory device having erase operation before program operation.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan T. Nguyen whose telephone number is (571) 272-1789. The examiner can normally be reached on Monday to Friday from 07:00 AM to 03:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho, can be reached at (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tan T. Nguyen
Primary Examiner
Art Unit 2827
August 04, 2005